CH7053A HDTV/VGA/ DVI Transmitter

FEATURES

- DVI Transmitter support up to 1080p
- DVI hot plug detection
- Supports Component YPrPb (HDTV) up to 1080p and analog RGB (VGA) monitor up to 1920x1080 resolution
- Supports DVI and VGA/HDTV output simultaneously
- Three 10-bit high speed DACs
- SPDIF audio interface supports either 16-bit or 20-bit stereo data for up to 192kHz/2ch
- Support 2 channel I2S digital audio input for up to 24-bit data stream (32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHzand 192kHz)
- TV/Monitor connection detect capability. DACs can be switched off through programming internal registers
- Pixel-level color enhancement for brightness, contrast, hue and saturation adjustment for HDTV output
- Supports 8/12/16/18/24-bit parallel interface input for either RGB format (RGB-565, RGB-666 or RGB-888 and etc.) or YCrCb format (ITU-R 656 or ITU-R 601). 80/86 MPU interface and DE only mode are also supported.
- Pixel clock input frequency support for up to 165 MHz
- IO Supply Voltages from 1.2V to 3.3V and SPC/SPD Supply Voltages from 1.8V to 3.3V.
- Programmable power management
- Device fully programmable through serial port
- Offered in a 88-pin QFN package

APPLICATION

- Media Internet Devices
- Media Storage Boxes
- Smart-books
- Digital Video Players
- Digital Video Recorders
- Portable Media Players

GENERAL DESCRIPTION

The Chrontel CH7053A is specifically designed for consumer electronics device and PC markets which multiple high definition content display formats are required. With its advanced video encoder, flexible scaling engine and easy-to-configure audio interface, the CH7053A satisfies manufactures' products display requirements and reduce their costs of development and time-to-market.

High quality high-bandwidth uncompressed video like DVI and YPrPb components or legacy VGA analog display are supported by the device's color format converter. The 3 high-performance, 10-bit DACs can be used for either HDTV display or VGA output depending on manufactures' products specification. The device is compliant with EIA770-3 and SMPTE 274M/293M/296M standards and supports HDTV resolution for up to 1080p. The CH7053A has the ability to generate composite syncs if required by the RGB monitor.

The CH7053A's 24-bit parallel bus accepts a wide range of input data formats from the graphic controller. The built-in video port supports 8/12/16/18/24-bit data interface as well as 80/86 MPU interface. The video format conversion module is capable of translating digital RGB-565, RGB-666, RGB-888 or YCrCb (ITU-R 656, ITU-R 601) signal to the DVI signal, combining with the audio stream. The input digital signal also can be transformed by the DACs for HDTV or VGA analog outputs.

The CH7053A supports both SPDIF and 2-channel I^{2}S digital audio input. Its high fidelity audio decoder engine has the capability of sampling audio frequency for up to 192k/2ch. The SPIDF supports PCM encoded data and compressed audio including Dolby Digital and DTS.

The CH7053A has an image enhancement function that can fine tune brightness, contrast, hue and saturation down to the pixel-level.

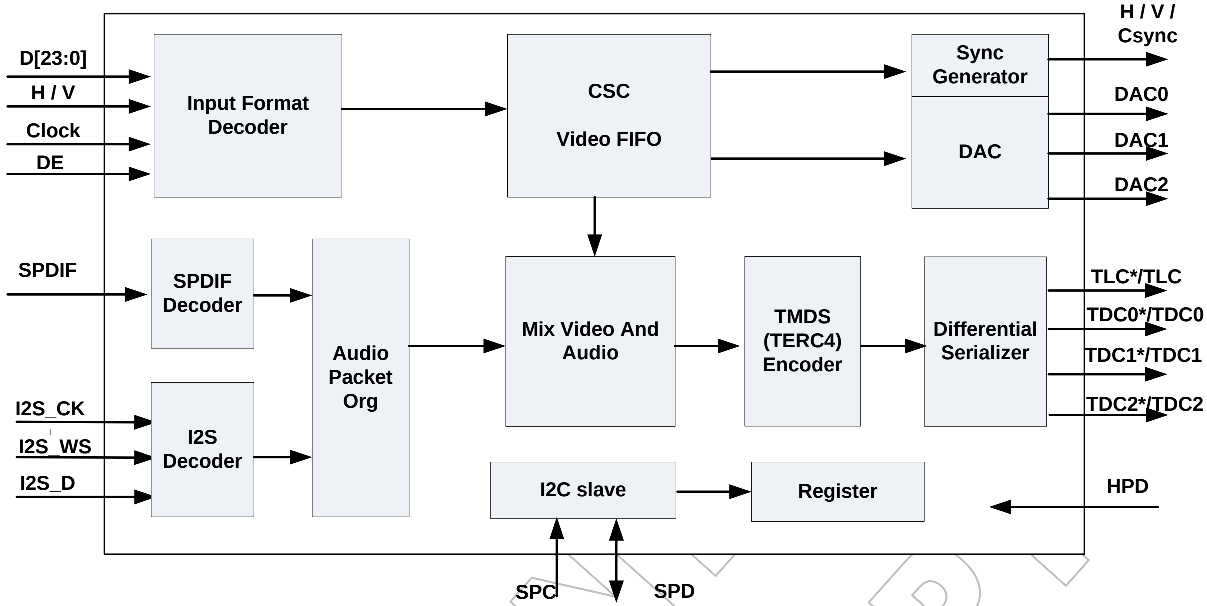

Figure 1: Functional Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

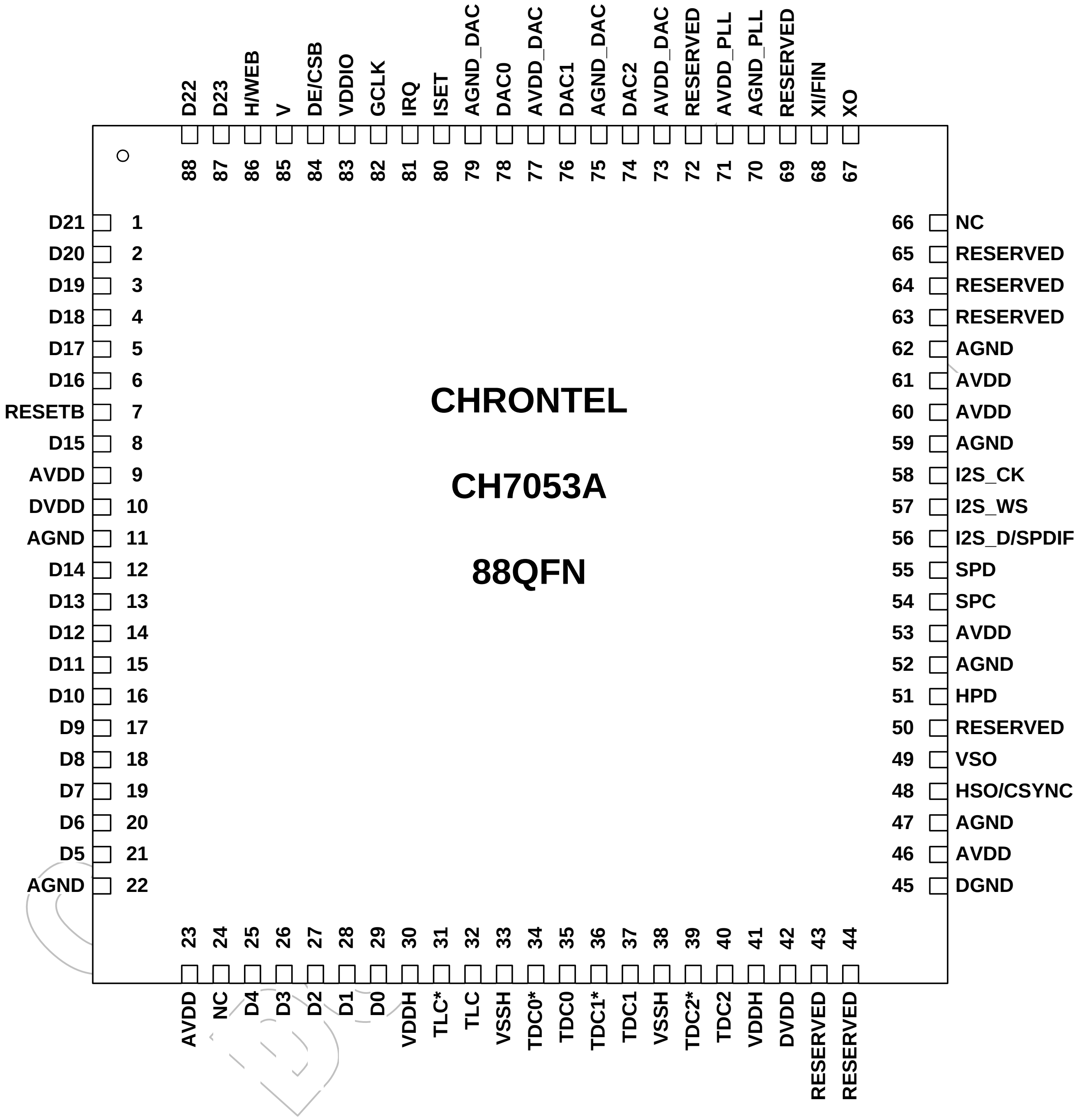

Figure 2: 88 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions (QFN88 Package)

Pin #	Type	Symbol	Description
1~6,8, 12~21, 25~29, 87~88,	In	D[23:0]	**Data Input** These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. All the unused Data input pins should be pulled low with 10KΩ resistors or shorted to Ground directly.
7	In	RESETB	**Reset Input** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
31,32	Out	TLC*,TLC	**DVI Clock Outputs** These pins provide the differential clock output for the DVI .
34,35	Out	TDC0*,TDC0	**DVI Data Channel 0 Outputs** These pins provide the DVI differential outputs for data channel 0
36,37	Out	TDC1*,TDC1	**DVI Data Channel 1 Outputs** These pins provide the DVI differential outputs for data channel 1
39,40	Out	TDC2*,TDC2	**DVI Data Channel 2 Outputs** These pins provide the DVI differential outputs for data channel 2
43	N/A	RESERVED	**Reserved** This pin should connect to DVDD directly
44	N/A	RESERVED	**Reserved** This pin should connect to DGND directly
48	Out	HSO/CSYNC	**Horizontal Sync Signal Output** The amplitude of this pin is from 0 to AVDD It also functions as a Composite sync output.
49	Out	VSO	**Vertical Sync Signal Output** The amplitude of this pin is from 0 to AVDD
50	N/A	RESERVED	**Reserved** This pin should be left open or pulled low with a 10 KΩ resistor in the application.
51	In	HPD	**Hot Plug Detect** This input pin determines whether the DVI output driver is connected to a DVI monitor. This pin should be pull low with 47 KΩ Resistor.
54	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required.
55	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required.
56	In	I2S_D/SPDIF	**I2S Data input or SPDIF Audio Signal Input** In default, this pin is configured to SPDIF audio signal input. The signal level is 0-2.5V. I2S audio input can be configured through programming CH7053A registers.
57	In	I2S_WS	**I2S Channel Select Signal**
58	In	I2S_CK	**I2S Clock Signal**
63,64,	N/A	RESERVED	**Reserved Pins** A pull-up resistor of 10 KΩ to 5V is needed
69,72	N/A	RESERVED	**Reserved Pins** A pull-up resistor of 10 KΩ to AVCC is needed

Pin #	Type	Symbol	Description
65	N/A	RESERVED	**Reserved Pins** A pull-low resistor 10 KΩ to ground is needed
24,66	N/A	NC	**Not Connected Pins**
67	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
68	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
74	Out	DAC2	**YPrPb or Analog RGB Output**
76	Out	DAC1	**YPrPb or Analog RGB Output**
78	Out	DAC0	**YPrPb or Analog RGB Output**
80	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
81	Out	IRQ	**Programmed Interrupt output**
82	In	GCLK	**External Clock Inputs** The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
84	In	DE/CSB	**Data Input Indicator** When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also a CSB signal input of MPU interface The amplitude will be 0V to VDDIO.
85	In/out	V	**Vertical Sync Input/Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
86	In/out	H/WEB	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of MPU interface.
9, 23,46, 53,60, 61	Power	AVDD	**Analog Power Supply (3.3V)**
10,42	Power	DVDD	**Digital Power Supply (1.8V)**
45	Power	DGND	**Digital Ground**
11,22,47,52, 59,62	Power	AGND	**Analog Ground**
30,41	Power	VDDH	**DVI Power Supply (3.3V)**
33,38	Power	VSSH	**DVI Ground**
71	Power	AVDD_PLL	**PLL Power Supply (1.8V)**
70	Power	AGND_PLL	**PLL Ground**

Pin #	Type	Symbol	Description
77,73	Power	AVDD_DAC	**DAC Power Supply (3.3V)**
75,79	Power	AGND_DAC	**DAC Ground**
83	Power	VDDIO	**IO supply voltage(1.2-3.3V)**

2.0 PACKAGE DIMENSIONS

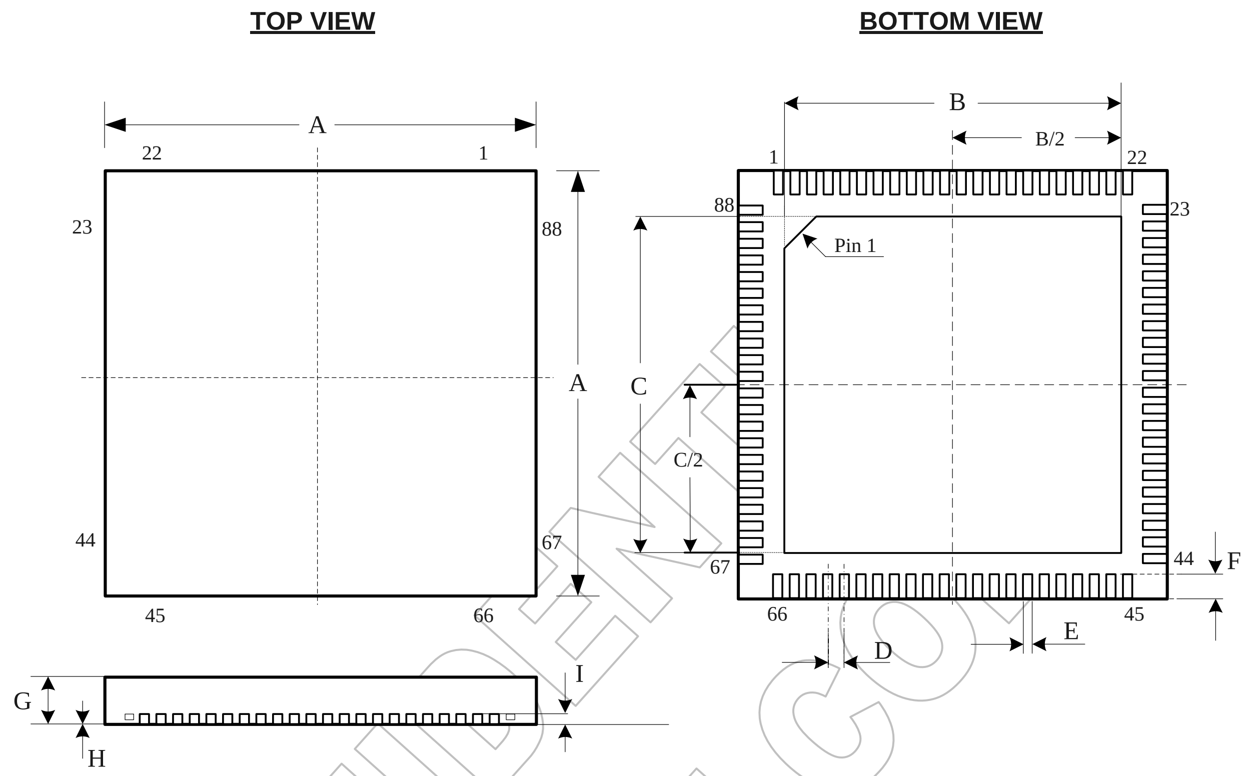

Figure 3: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		**SYMBOL**								
88 (10 X 10 mm)		**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**
Milli-meters	**MIN**	**9.90**	**6.60**	**6.60**	**0.4**	**0.15**	**0.35**	**0.8**	**0**	**0.20**
	MAX	**10.10**	**6.90**	**6.90**		**0.25**	**0.60**	**0.9**	**0.05**	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7053A-BF	88QFN, Lead-free	Commercial : -20 to 70°C	168/Tray
CH7053A-BFI	88QFN, Lead-free	Industrial : -40 to 85°C	168/Tray

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